Scalability with conveyor-belt spin-qubit shuttling in Si/SiGe

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Conveyor-mode shuttling transports a spin qubit adiabatically while it remains confined in a propagating sinusoidal potential defined by gate electrodes in a quantum channel [1]. A central advantage of this approach is its purely electrical operation requiring only a few easily tunable control signals [2], and its compatibility with industrial gate-fabrication processes [3]. Crucially, the electron spin encoding the qubit can be preserved during transport in Si/SiGe [4]. Mobile spin qubits enable new schemes for qubit manipulation and readout, and they offer a pathway to reducing spin-qubit cross-talk and heating.

I discuss our concept for integrating mobile qubits into sparse quantum-computing architectures [5], enabling co-integration with cryogenic electronics [6]. To fully harness the capabilities of spin-qubit shuttling, linear shuttle lanes must be extended into a two-dimensional grid with controllable routing. I show how T-junctions between shuttle lanes can be realized without introducing additional control lines [7]. I further discuss experimental insights into how inhomogeneities in the Si/SiGe heterostructure influence conveyor-mode spin-qubit shuttling [8]. A key feature of the conveyor-mode approach is that the shuttling process itself can be used to map local material properties such as electrostatic disorder, valley splitting [9] and valley phase [10]. These spatial maps provide valuable feedback for mitigation strategies and for benchmarking material-improvement efforts, including strain engineering and Ge-composition modulation [11].

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